AMENDMENTS TO THE CLAIMS

This listing of claims will replace all prior versions, and listings, of claims in the application:

1. (original) Apparatus for processing data, said apparatus comprising:

a process core (4) operable to execute data processing instructions to generate result data values; and

data processing registers (12) holding data values defining state of said processor core to which said result data values are written; wherein

at least one data processing instruction executed by said processor core is a conditional write data processing instruction encoding condition codes (26) specifying conditions under which said conditional write data processing instruction will or will not be permitted to write data to effect a change in state of said processor core: and further comprising

a trash register (51) to which a result data value may be written instead of a data processing register upon execution of said conditional write data processing instruction when said condition codes within said conditional write data processing instruction do not permit a write to effect a change in state of said processor core.

2. (original) Apparatus as claim in claim 1, comprising a register bank (12) having a plurality of data registers to which result data values are written.

3. (currently amended) Apparatus as claimed in ~~any one of the preceding claims~~ claim 1, wherein writing to said trash register (51) is programmably disabled by a trash register control signal.

4. (original) Apparatus as claimed in claim 3, wherein said trash register control signal is stored in a system configuration register.

5. (original) Apparatus as claimed in claim 2, wherein said trash register (51) is part of said register bank, said trash register being unmapped to a register number such that said trash register may not be specified by a register specifying operand value.

6. (original) A method of processing data, said method comprising the steps of:

generating result data values upon execution by a processor core (4) of data processing instructions, at least one data processing instruction executed being a conditional write data processing instruction encoding condition codes (26) specifying conditions under which said conditional write data processing instruction will or will not be permitted to write data to effect a change in state of said processor core and wherein

a result data value is not written to a data processing register holding a data value defining state of said processor core when condition codes within said condition write data processing instruction do not permit a write to effect a change in state of said processor core but is instead written to a trash register (51).

7. (original) A method as claimed in claim 6, wherein said data processing register is part of a register bank (12) having a plurality of data registers to which result data values are written.

8. (currently amended) A method as claimed in ~~any one of claim 6 and 7~~ claim 6, wherein writing to said trash register (51) is programmable disabled by a trash register control signal.

9. (original) A method as claimed in claim 8, wherein said trash register control signal is stored in a system configuration register.

10. (original) A method as claimed in claim 7, wherein said dummy register is part of said register bank, said trash register being unmapped to a register number such that said trash register may not be specified by a register specifying operand value.